CLAIMS

What is Claimed is:

1 (Cancelled).

2 (Cancelled).

3 (Cancelled).

4 (Cancelled).

5 (Cancelled).

6 (Cancelled).

7 (Cancelled).

8 (Cancelled).

9 (Cancelled).

10 (Cancelled).

11 (Cancelled).

12 (Cancelled).

13 (Cancelled).

14 (Cancelled).

15 (Cancelled).

16 (Cancelled).

17 (Cancelled).

18 (Cancelled).

19 (Cancelled).

20 (Cancelled).

21(Previously Presented) A high speed serial memory interface system comprising:

an information configuration core for coordinating proper alignment of information communication signals, wherein said information configuration core includes a transmit channel with:

a phase aligner for aligning signals forwarded from said memory array interface;

an encoder for encoding said signals forwarded from said memory array interface, said encoder coupled to said phase aligner; and

a serializer for serializing signals receive from said memory array interface, said serializer coupled to said encoder;

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core; and

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core, wherein said memory array is included on a same substrate as said high speed serial memory interface system.

22. (Cancelled).

23. (New) A high speed serial memory interface system of claim 21 wherein said memory array interface operates at a second clock speed that is slower than a first clock speed of operations at said system interface.

24. (New) A high speed serial memory interface system of claim 21 wherein said memory array interface deals with the reading and writing of data to and from a memory array with the address and control buses.

25. (New) A high speed serial memory interface system of claim 21 wherein said communications are synchronous to a system clock at double rated clocking.

26. (New) A high speed serial memory interface system of claim 21 wherein said system interface includes a serial memory interface that operates at a first clock speed that is faster than a second clock speed of operations at said memory array interface.

27. (New) A high speed serial memory interface system of claim 21 wherein said information configuration core includes 8B/10B encoding.

28. (New) A high speed serial memory interface system of claim 21 wherein a memory module array is coupled by lines internal in a single substrate to said high speed serial memory interface system without drivers.

29. (New) A high speed serial memory interface system of claim 21 wherein data and address bits are provided synchronously upon a clock signal edge.

30. (New) A high speed serial memory interface system comprising:

an information configuration core for coordinating proper alignment of information communication signals, wherein said information configuration core includes a receive channel with:

a deserializer for deserializing information received from said system interface;

a framer for framing information received from said system interface to its byte boundary, said framer coupled to said deserializer;

a decoder for decoding information received from said system interface, said decoder coupled to said framer; and

an elasticity buffer for buffering information received from said system interface, said elasticity buffer coupled to said decoder;

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core; and

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core, wherein said memory array is included on a same substrate as said high speed serial memory interface system.

31. (New) A high speed serial memory interface system of claim 30 wherein said memory array interface operates at a second clock speed that is slower than a first clock speed of operations at said system interface.

32. (New) A high speed serial memory interface system of claim 30 wherein said memory array interface deals with the reading and writing of data to and from a memory array with the address and control buses.

33. (New) A high speed serial memory interface system of claim 30 wherein said communications are synchronous to a system clock at double rated clocking.

34. (New) A high speed serial memory interface system of claim 30 wherein said system interface includes a serial memory interface that operates at a first clock speed that is faster than a second clock speed of operations at said memory array interface.

35. (New) A high speed serial memory interface system of claim 30 wherein said information configuration core includes 8B/10B encoding.

36. (New) A high speed serial memory interface system of claim 30 wherein a memory module array is coupled by lines internal in a single substrate to said high speed serial memory interface system without drivers.

37. (New) A high speed serial memory interface system of claim 30 wherein data and address bits are provided synchronously upon a clock signal edge.